

What is claimed is:

1           1.           An apparatus comprising:  
2           a register stack engine to trigger memory operations in support of register windows;  
3           the register stack engine further to generate one or more micro-operations to perform a  
4           register window operation.

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1           2.           The apparatus of claim 1, wherein:  
2           the register stack engine is further to insert the one or more micro-operations into an  
3           execution pipeline.

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1           3.           The apparatus of claim 1, wherein:  
2           the register window operation is a spill operation.

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1           4.           The apparatus of claim 3, wherein:  
2           the one or more micro-operations include a store micro-operation.

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1           5.           The apparatus of claim 1, wherein:  
2           the register window operation is a fill operation.

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1        6.        The apparatus of claim 5, wherein the one or more micro-operations include a  
2                    load micro-operation.

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1        7.        The apparatus of claim 1, wherein:  
2                    the register stack engine is further to generate the micro-operations indirectly, via a  
3                    micro-op generator.

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1        8.        The apparatus of claim 2, wherein:  
2                    the register stack engine is further to insert the one or more micro-operations into the  
3                    execution pipeline indirectly, via a micro-op generator.

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1        9.        The apparatus of claim 2, further comprising:  
2                    a micro-operation queue;  
3                    wherein inserting the one or more micro-operations into the execution pipeline further  
4                    comprises inserting the micro-operations into the micro-operation queue.

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1        10.        The apparatus of claim 1, wherein:  
2                    the register window operation is associated with an implicit operand; and  
3                    the one or more micro-operations includes a micro-operation that indicates the implicit  
4                    operand as an explicit operand.

1 11. The apparatus of claim 10, wherein:

2 the implicit operand is a status bit collection register.

1 12. The apparatus of claim 10, wherein:

2 the implicit operand is a store pointer register.

1 13. The apparatus of claim 10, wherein:

2 the implicit operand is a load pointer register.

1 14. The apparatus of claim 1, further comprising:

2 a scheduler to schedule the micro-operations for execution;

3 wherein the scheduler is to concurrently consider the register window operation micro-  
4 operations as well as other micro-operations in an out-of-order scheduling scheme.

1 15. The apparatus of claim 1, wherein:

2 each of the micro-operations is of a format that includes a single explicit destination  
3 operand and two explicit source operands.

1 16. A system comprising:

2 a memory to store an instruction, the memory including a backing store to store one or  
3 more spilled values; and

4 a processor coupled to the memory;

5 wherein the processor includes a register stack engine to generate, responsive to the  
6 instruction, one or more micro-operations to cause a register stack operation.

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1 17. The system of claim 16, wherein:

2 the memory is a DRAM.

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1 18. The system of claim 16, wherein:

2 the processor further includes an architectural renamer to rename registers to support  
3 register windowing.

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1 19. The system of claim 16, wherein:

2 the processor further includes an out-of-order rename unit to map logical registers to  
3 physical registers in order to increase parallelism.

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1 20. The system of claim 16, wherein:

2 the register stack operation is a spill operation.

1        21.        The system of claim 16, wherein:  
2                the register stack operation is a fill operation.

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1        22.        The system of claim 16, wherein:  
2                the processor further includes a scheduler to perform out-of-order scheduling for a set of  
3                micro-operations, wherein the set of micro-operations includes a regular micro-operation and  
4                also includes the one or more micro-operations to cause a register stack operation.

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1        23.        The system of claim 22, wherein:  
2                the scheduler considers the set of micro-operations for out-of-order scheduling such that  
3                the regular micro-operation and the one or more micro-operations are scheduled in an  
4                intermingled fashion.

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1        24.        A method comprising:  
2                performing an architectural rename stage for an instruction, in order to support register  
3                windowing; and  
4                performing an out-of-order rename stage for each of the one or more micro-operations.

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1        25.        The method of claim 24 wherein:  
2                the instruction is a procedure call instruction to invoke a new procedure; and

3 performing an architectural rename stage further comprises renaming physical register  
4 operands for a current procedure such that output registers for the current procedure are  
5 identified as input registers for the new procedure .

1 26. The method of claim 24 wherein:

2 performing an architectural rename stage further comprises renaming a first input register  
3 to a predetermined physical register number.

1 27. The method of claim 24, further comprising:

2 generating one or more micro-operations to implement the instruction.

1 28. The method of claim 27 wherein:

2 generating one or more micro-operations further comprises generating a micro-op to  
3 perform a desired memory operation.

1 29. The method of claim 27 wherein:

2 generating one or more micro-operations further comprises generating a micro-op to  
3 perform an arithmetic operation associated with a register stack engine ("RSE") operation.

1 30. The method of claim 27 wherein:

2 generating one or more micro-operations further comprises generating a micro-op to  
3 perform a bit manipulation operation associated with a register stack engine ("RSE")  
4 operation.

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1 31. The method of claim 24 wherein:

2 performing an out-of-order rename stage further comprises mapping an architectural  
3 register to a physical rename register in order to minimize data dependencies.

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1 32. A method, comprising:

2 generating one or more micro-operations to perform a RSE operation; and  
3 inserting the one or more micro-operations into an execution pipeline;  
4 wherein the RSE operation is to support register windowing.

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1 33. The method of claim 32, wherein:

2 the RSE operation is a spill operation ; and  
3 generating one or more micro-operations further comprises generating a store micro-  
4 operation.

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1 34. The method of claim 33, wherein:

2       generating a store micro-operation further comprises generating a store micro-operation  
3       to store data associated with the spill operation to a backing store in a memory.

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1       35.       The method of claim 32, wherein:

2       generating one or more micro-operations further comprises generating a micro-operation  
3       to operate on an implicit operand.

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1       36.       The method of claim 35, wherein:

2       generating one or more micro-operations further comprises generating a micro-operation  
3       to perform an arithmetic operation on an implicit operand.

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1       37.       The method of claim 35, wherein:

2       generating one or more micro-operations further comprises generating a micro-operation  
3       to perform a bit-manipulation operation on an implicit operand.

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1       38.       The method of claim 35, wherein:

2       the implicit operand is a status bit collection register.

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1       39.       The method of claim 35, wherein:



2 generating a micro-operation to operate on an implicit operand further comprises  
3 generating a micro-operation to collect a status bit into the implicit operand.

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1 40. The method of claim 35, wherein:

2 generating a micro-operation to operate on an implicit operand further comprises  
3 generating a micro-operation to restore a status bit value from the implicit operand.

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1 41. The method of claim 32, wherein:

2 the RSE operation is a fill operation; and  
3 generating one or more micro-operations further comprises generating a load micro-  
4 operation.

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1 42. The method of claim 41, wherein:

2 generating a load micro-operation further comprises generating a load micro-operation to  
3 load data associated with the fill operation from a backing store in a memory into a register.

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1 43. The method of claim 32, wherein:

2 the RSE operation is a spill operation; and  
3 generating one or more micro-operations further comprises generating a micro-operation  
4 to assign data associated with the spill operation to one half of a double-wide data register.

1        44.        The method of claim 43, further comprising:

2            generating one or more micro-operations to store the contents of the double-wide data  
3        register to a backing store.

1        45.        The method of claim 43, wherein generating one or more micro-operations further  
2            comprises:

3            determining whether a pre-determined number of prior spill operations has been  
4        performed;

5            if not, generating a micro-operation to assign general register data to the one half of a  
6        double-wide data register value; and

7            otherwise, generating a micro-operation to assign status data to the one half of the  
8        double-wide data register.

1        46.        The method of claim 45, further comprising:

2            if the pre-determined number of prior spill operations has not been performed, generating  
3        a micro-operation to merge a status bit into a status collection variable.

1        47.        The method of claim 45, further comprising:

2            generating one or more additional micro-operations to perform a second spill operation;

3            wherein generating the one or more additional micro-operations includes:

4           generating a micro-operation to assign general register data to the other half of the  
5           double-wide data register; and  
6           generating a micro-operation to store the double-wide data register value to a backing  
7           store.

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1       48.       The method of claim 47, wherein generating one or more additional micro-  
2           operations further comprises:

3           generating the micro-operation to assign general register data to the other half of the  
4           double-wide data register only if a predetermined number of prior spill operations has  
5           occurred;

6           otherwise, generating a micro-operation to assign status data to the other half of the  
7           double-wide data register.

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1       49.       The method of claim 32, wherein:

2           the RSE operation is a fill operation; and

3           generating one or more micro-operations further comprises generating a micro-operation  
4           to obtain a double-wide data value from a backing store.

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1       50.       The method of claim 49, further comprising:

2           generating one or more micro-operations to assign one half of the double-wide data value  
3           to a general register.

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1 51. The method of claim 49, further comprising:

2 generating one or more micro-operations to assign one half of the double-wide data value  
3 to a status bit collection register.

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1 52. The method of claim 49, wherein generating one or more micro-operations further  
2 comprises:

3 determining whether a pre-determined number of prior fill operations has been  
4 performed;

5 if not, generating a micro-operation to assign one half of the double-wide data register  
6 value to a general register; and

7 otherwise, generating a micro-operation to assign one half of the double-wide data  
8 register value to a status collection register.

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1 53. The method of claim 52, further comprising:

2 if the pre-determined number of prior fill operations has not been performed, generating a  
3 micro-operation to extract a status bit from a status collection register.

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1 54. The method of claim 52, further comprising:

2 generating one or more additional micro-operations to perform a second fill operation;

3 wherein generating the one or more additional micro-operations includes:

4 generating a micro-operation to assign the other half of the double-wide data register  
5 data to a general register.

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1 55. The method of claim 54, wherein generating one or more additional micro-  
2 operations further comprises:

3 generating the micro-operation to assign a general register to the other half of the double-  
4 wide data register value only if a predetermined number of prior fill operations has occurred;  
5 otherwise, generating a micro-operation to assign the other half of the double-wide data  
6 register to a status collection register.

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1 56. A method comprising:

2 generating micro-operations to perform, in a single cycle, M parallel memory operations  
3 in support of register windowing, where  $M > 1$ ;

4 wherein generating micro-operations further comprises:

5 utilizing a first memory pointer register to determine the memory address for a  
6 first memory operation; and

7 utilizing a second memory pointer register to determine the memory address for a  
8 second memory operation.

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1 57. The method of claim 56, wherein generating micro-operations further comprises:

utilizing an Nth memory pointer register to determine the memory address for the Nth memory operation.

58. The method of claim 56, wherein:

the first and second memory pointer registers provide memory addresses for store operations.

59. The method of claim 56, wherein:

the first and second memory pointer registers provide memory addresses for load instructions.

60. The method of claim 58, further comprising:

incrementing the values of the first and second memory pointer registers by  $M \cdot x$ , where  $x$  is the size of the data to be stored during each of the store operations.

61. The method of claim 59, further comprising:

decrementing the values of the first and second memory pointer registers by  $M \cdot x$ , where  $x$  is the size of the data to be loaded during each of the load operations.